

## CLAIMS

We claim:

1     **1**     A system that converts words of pipelined data from a first data width to a  
2 smaller data width over series of cycles, comprising:  
3         a pipeline control that generates a word that is at least twice as wide as the  
4 smallest data width and shifts the pipelined data within the generated word such that  
5 the pipelined data word is, depending on the cycle, either prefixed by zeros, suffixed by  
6 zeros, or both, and that outputs a residual portion that is at least as wide as the smaller  
7 data width and a current portion that is at least as wide as the smaller data width;  
8         a delay register that receives at least a portion of the residual portion of the data  
9 from the pipeline control and delays the received residual portion one cycle from the  
10 current portion of the data from the pipeline control;  
11         a combinator circuit that compares the delayed residual portion of data from the  
12 delay register with the current portion of data from the pipeline control, and outputs  
13 data having a width equal to the smaller data width; and  
14         output conduits that, for every complete series, transport  
15             the current portion of the data during the initial cycle;  
16             the combinator circuit output during the non-initial cycles; and  
17             the residual portion of the data during the final cycle.

1    2    The system of claim 1, wherein:  
2        the first data width is 66 bits;  
3        the second data width is 64 bits; and  
4        the series repeats itself every 32 cycles.

1    3    The system of claim 1, wherein the system is used in an interface circuit.

1    4    The system of claim 1, wherein:  
2        the cycle is identified by a cycle value; and  
3        the pipeline control includes:  
4            a plurality of shift control circuits for a shifting the pipelined data, each  
5            shift control circuit shifting the data a different amount and being controlled by  
6            the cycle value.

1    5    The system of claim 1, wherein:  
2        the cycle is identified by a cycle value; and  
3        the pipeline control includes:  
4            a plurality of shift control circuits for a shifting the pipelined data, each  
5            shift control circuit shifting the data a different amount and being controlled by  
6            the cycle value, the amount being shifted being an exponential function.

6 The system of claim 1, further comprising a multiplexor that, in the initial cycle  
of every series, disregards the result from the combinator circuit and directs the current  
portion of the data to the output conduit.

7 The system of claim 1, further comprising a zero-loading circuit that, in the initial  
cycle of every series, replaces the inputs to the combinator circuit with the current portion  
of data from the pipeline control and zeros such that the output will equal the current  
portion of the data, and can be directed to the output conduit.

8 A system that converts pipelined data from a first data width to a smaller data  
width over series of cycles, comprising:

a pipeline control that, depending on the cycle, outputs a residual portion and a  
current portion;

a delay register that receives the residual portion of the data from the pipeline  
control and delays the received residual portion one cycle from the current portion of  
the data from the pipeline control;

a combinator circuit that compares the delayed residual portion of data from the  
delay register with the current portion of data from the pipeline control, and outputs  
data; and

a flow-through logic circuit that outputs data having a width that is at least as  
wide as the smaller data width from the pipelined data in the first cycle in which data is  
outputted of every series.

1 9 A transmitting interface comprising:

2 a system that encapsulates a data stream and prepares the encapsulated data

3 stream for transmission over an optical network, including:

4 a system that encapsulates the data stream;

5 a system that system that converts the encapsulated data stream from a

6 first data width to a smaller data width over series of cycles, including:

7 a pipeline control that, depending on the cycle, shifts encapsulated

8 data and outputs a residual portion that is at least as wide as the smaller data width and

9 a current portion that is at least as wide as the smaller data width;

10 a delay register that receives at least a portion of the residual

11 portion of the data from the pipeline control and delays the received residual portion

12 one cycle from the current portion of the data from the pipeline control;

13 a combinator circuit that compares the delayed residual portion of

14 data from the delay register with the current portion of data from the pipeline control,

15 and outputs data having a width equal to the smaller data width; and

16 a flow-through logic circuit that outputs data having a width that is

17 at least as wide as the smaller data width from the pipelined data in the first cycle in

18 which data is outputted of every series; and

19 a system that prepares outputted data for conversion to optical signals;

20 a system that serializes data streams that are encapsulated and prepared for

21 conversion to optical signals; and

22 a system that transmits optical signals.

1 10 A method of converting a series of input data words of a first data width to a  
2 series of output data words of a smaller data width, concatenation of the series of input  
3 data being equivalent to concatenation of the series of output data, the series having a  
4 sequence including an initial sequence, a non-initial sequence, a final sequence and a  
5 non-final sequence, comprising:

6 identifying a first portion and a second portion of each input data word, the size  
7 of each portion depending on the progression of the input series, the size of the first  
8 portion initially having a size equal to the smaller data width, gradually decreasing as  
9 the input series progresses, and the size of the second portion gradually increasing until  
10 the size is equal to the smaller data width when the input series is completed;

11 delaying the second portion of each input data word for at least the non-final  
12 sequences of each input series;

13 combining the delayed second portion with the first portion for at least the non-  
14 initial sequences of each input series;

15 outputting the first portion for the initial sequence of each output series;

16 outputting the combination for at least the non-initial and non-final sequences of  
17 each output series; and

18 outputting the second portion for the final sequence of each completed output  
19 series.

1   **11**    The method of claim 10, wherein:  
2           the first data width is 66 bits;  
3           the second data width is 64 bits; and  
4           each series has a maximum of 32 increments of ordered data words.

1   **12**    The method of claim 11, wherein the size of the first portion decreases by 2 bits  
2   and the size of the second portion increases by 2 bits for every increment.

1   **13**    The method of claim 12, wherein the system is used in an interface circuit.